Running Verilog-HDL file – tutorial using Vivado 2017.3

LSI Design Contest 2018

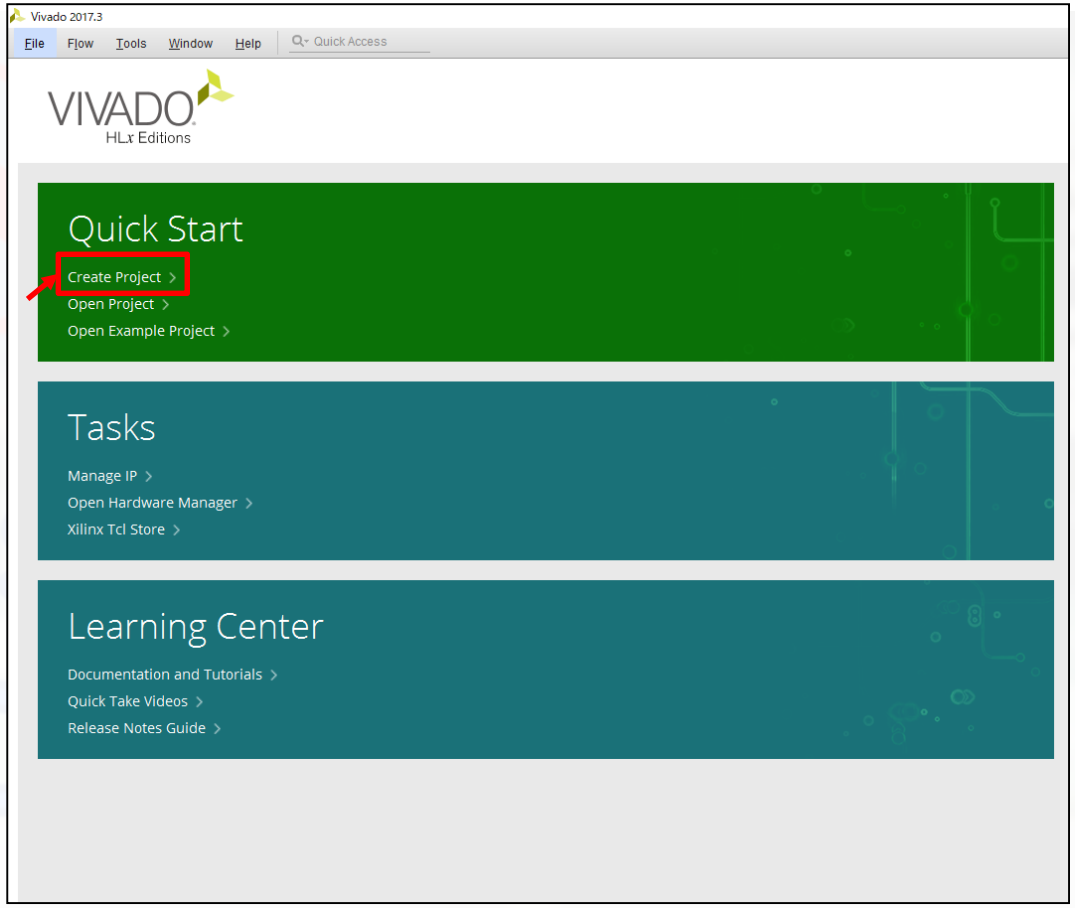
Adding zybo board package

- Download zybo board files from the link below:
  - https://reference.digilentinc.com/reference/software/vivado/board-files
- Unarchive the file
  - Copy all the board files from the folder
    - ¥vivado-boards-master¥new¥board_files
  - Paste the board files to your installed vivado path directory
    - C:¥Xilinx¥Vivado¥2017.3¥data¥boards¥board_files

Opening Vivado

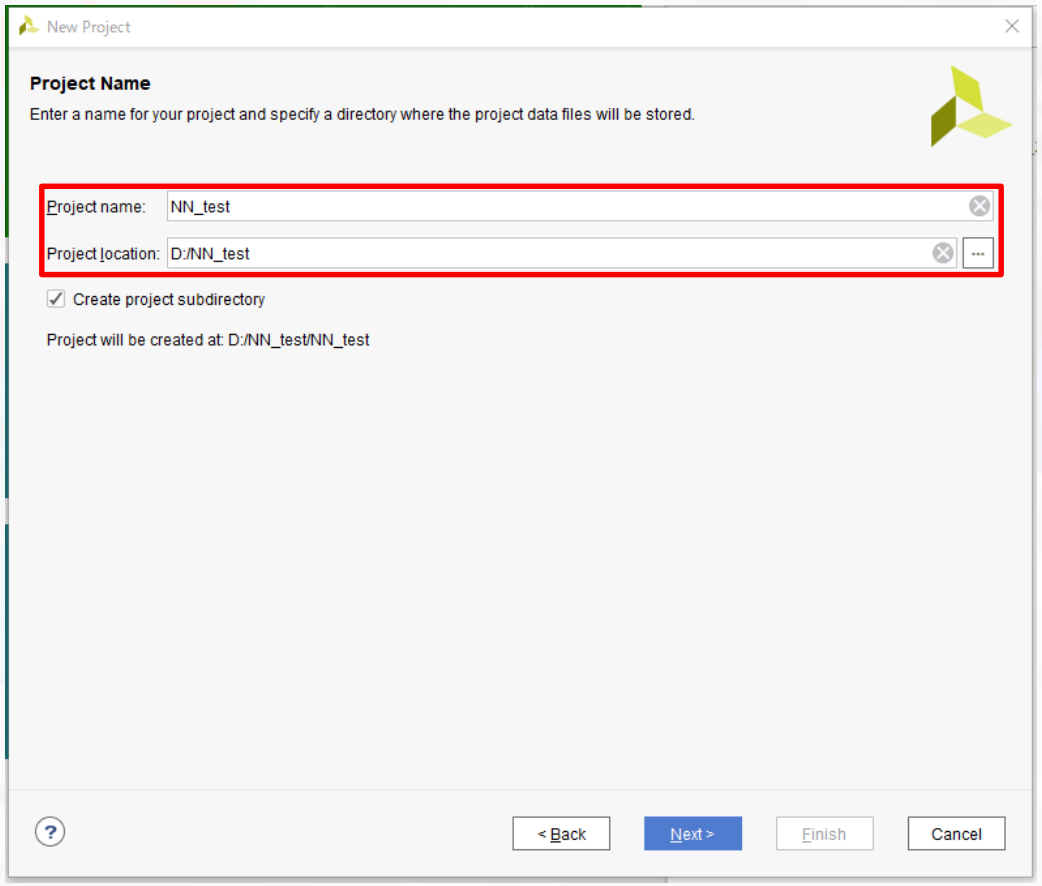
- Open Vivado
  - Note that the version used here is 2017.3

  - Next, click the「Create Project…」as shown in the figure.



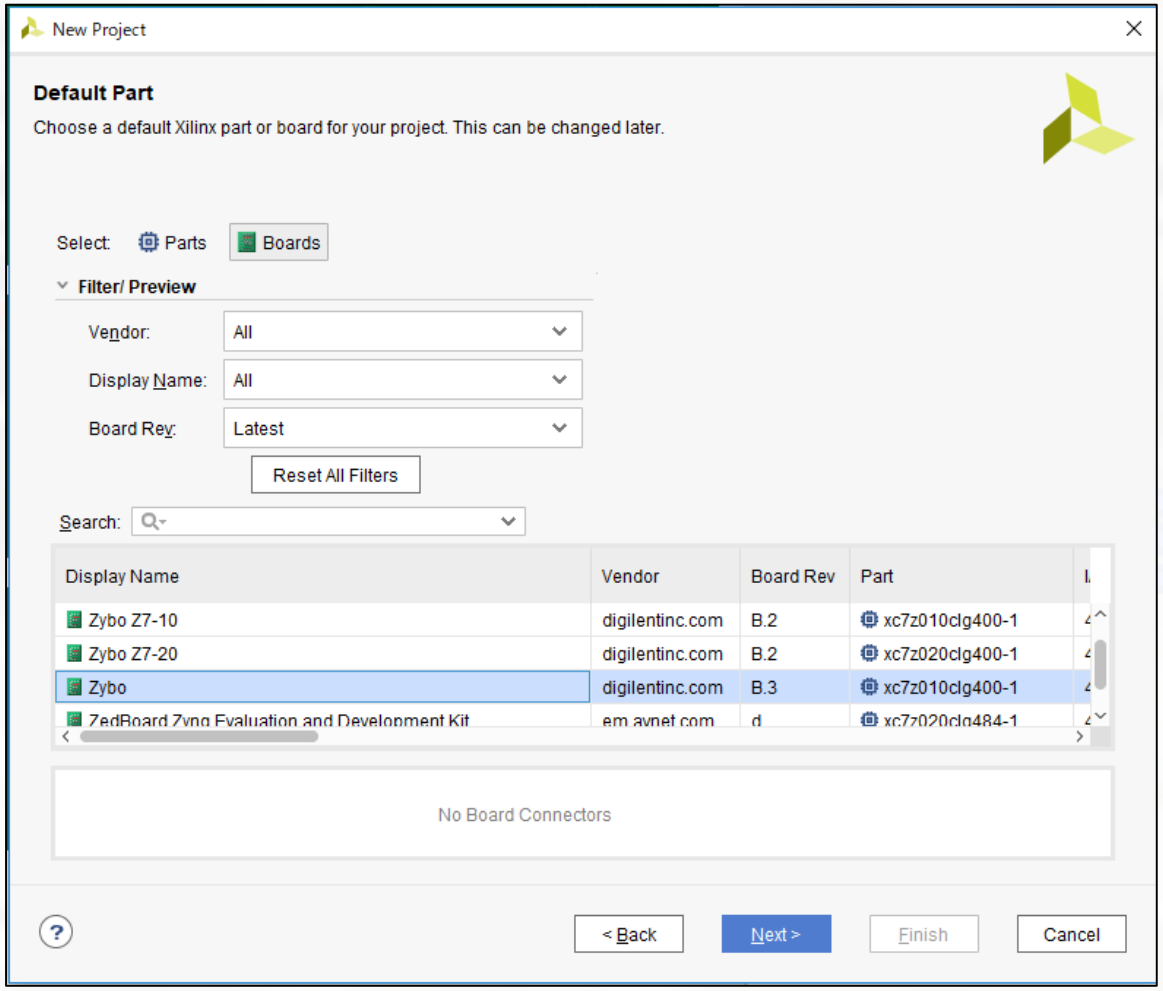
Locating project file

- Create a New Vivado project will come out, clik next.
- Assign the location to your selected folder
- Enter the name
  - For example : NN_test
- Click, next
- Project type terminal will come out
  - click next
- Add Sources terminal will come out
  - click next
- Add Constraints terminal will come out
  - click next
- Default part terminal will come out
  - select your specified boards
  - and finish.



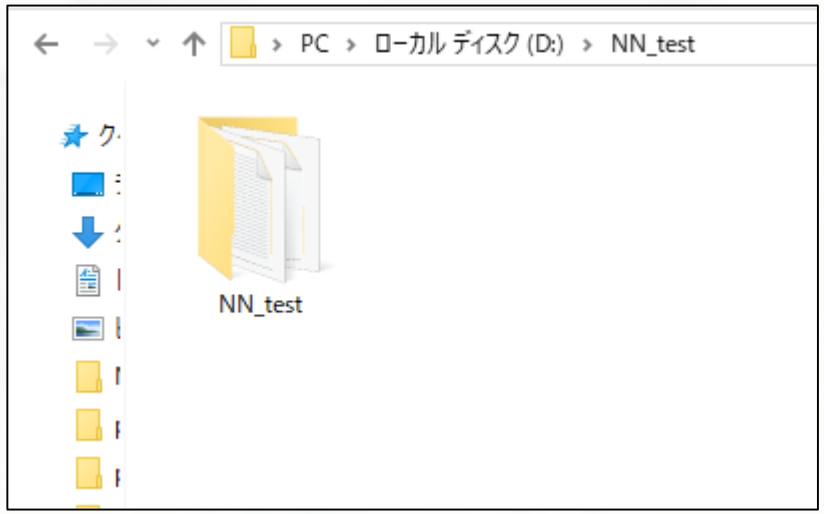
Specifying board

- Default part terminal will come out
  - select your specified boards
  - click next
- Click finish.

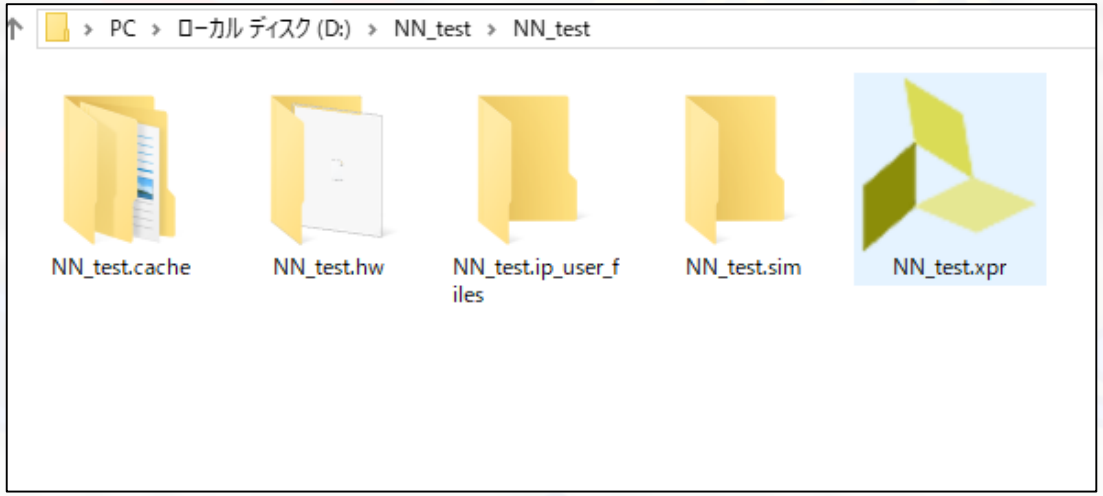


Locating project file

- A new folder will be created in your selected location

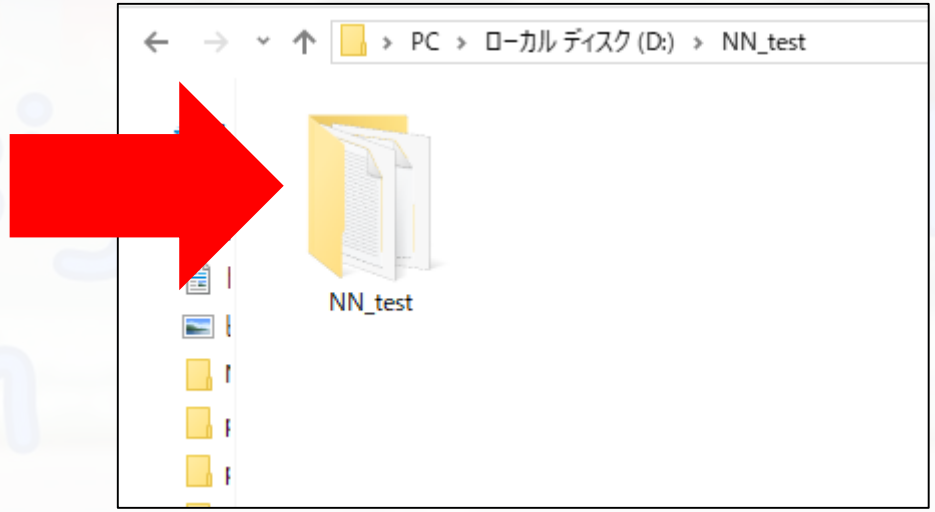


contents



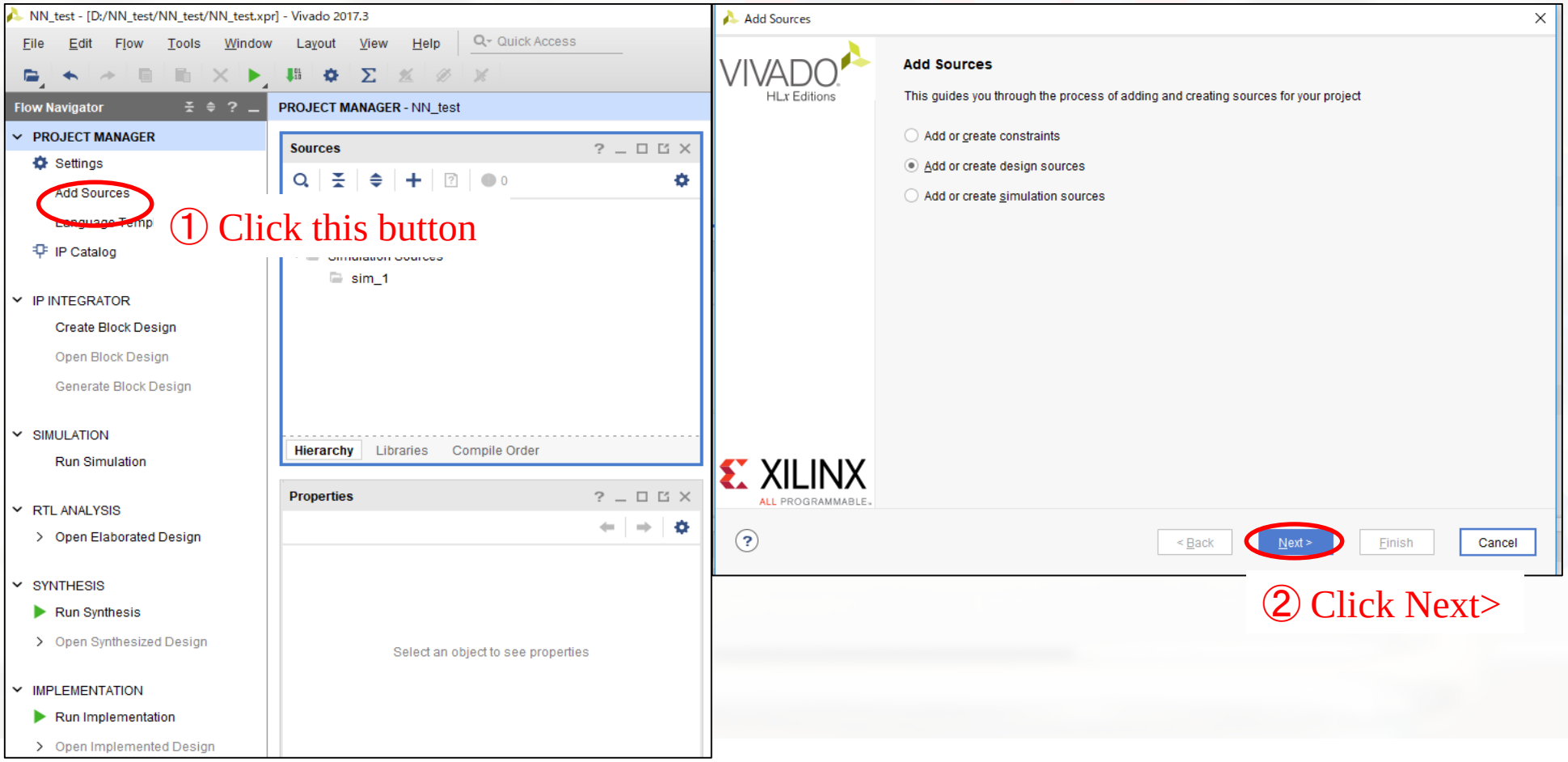
Download Verilog file

- Download the zip file from LSI design contest HP.
  - Link : http://www.lsi-contest.com/shiyou_4e.html
    - (Verilog file for simulation)
- Extract the file
  - There will be around 45 Verilog file
- Move all the Verilog file into NN_test folder



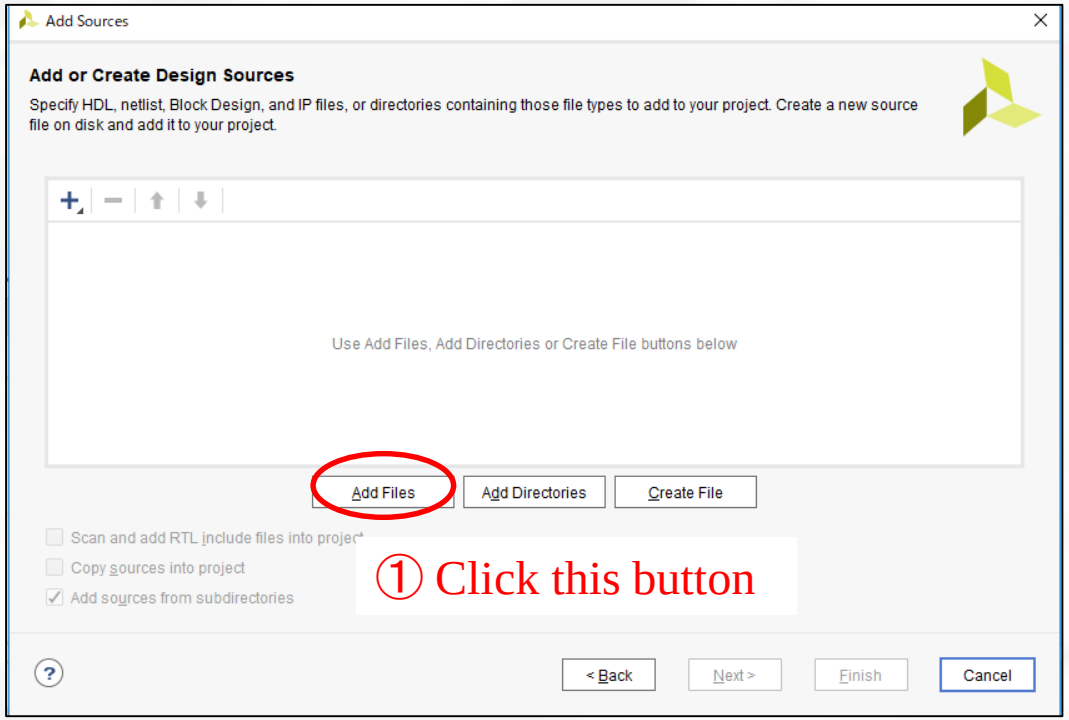
Add source file

- Click Add source

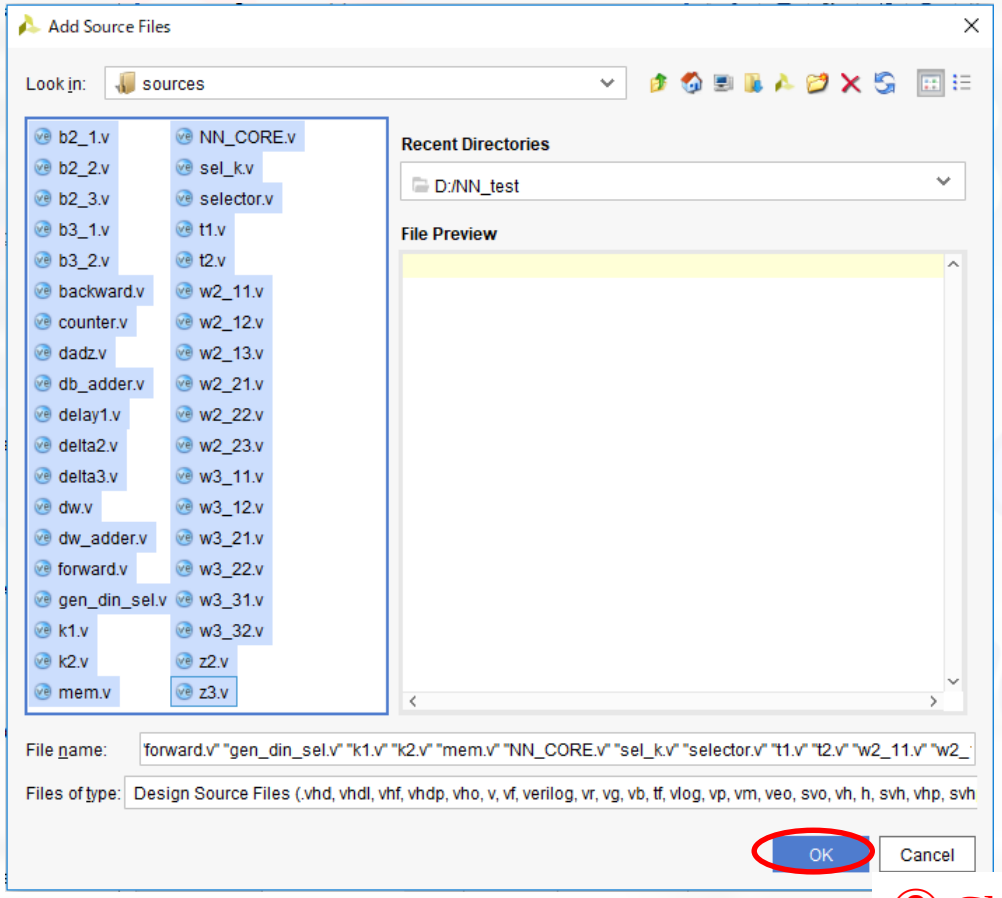


Add source file

- Click Add file
  - Go to folder ‘sources’ directory
  - Select all the files



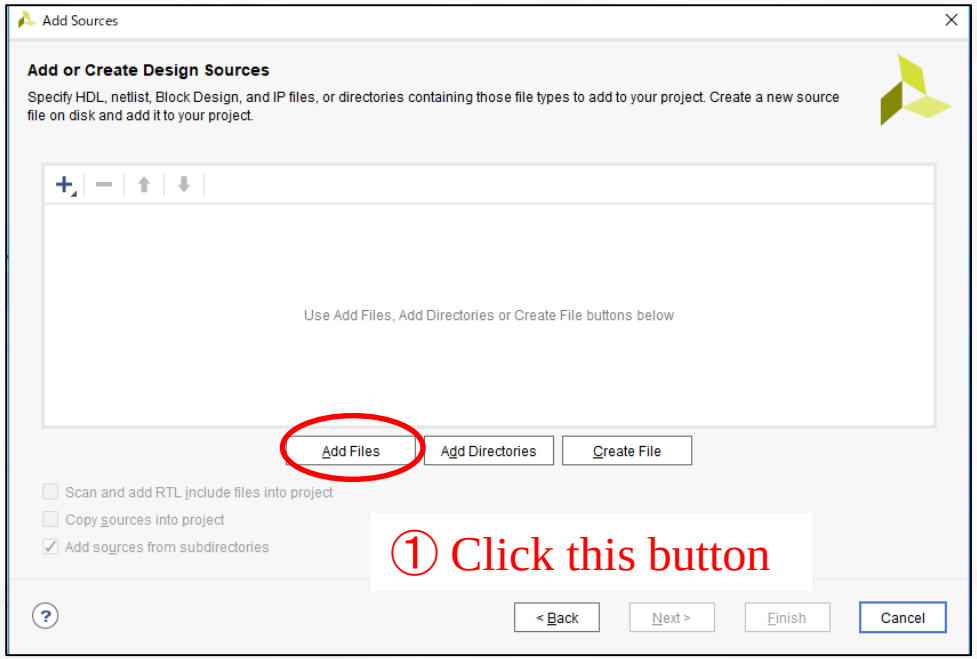
① Click this button



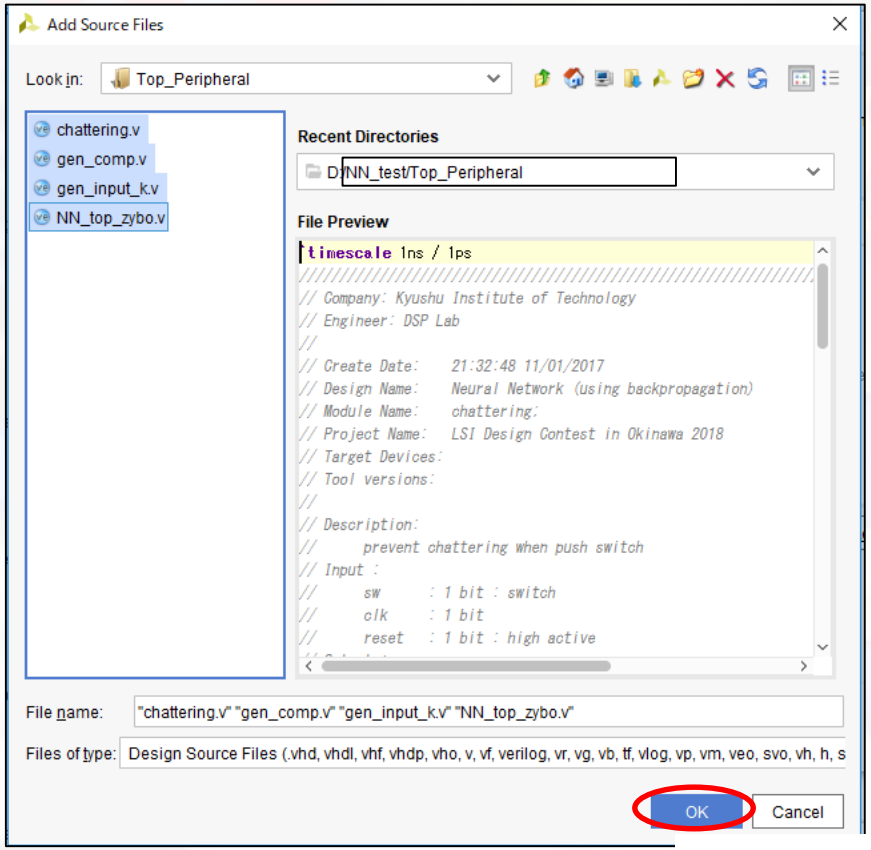
② Click OK, then Finish

Add source file

- Click Add file
  - Go to folder ‘Top_Peripheral’ directory
  - Select all the files



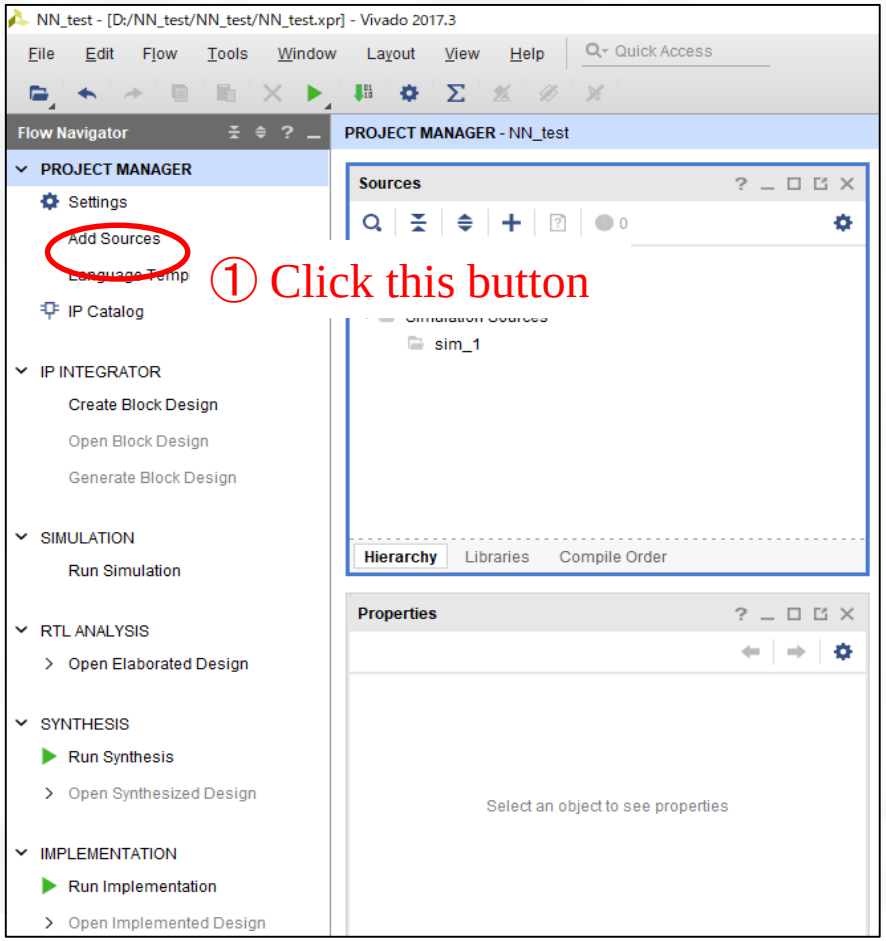
① Click this button

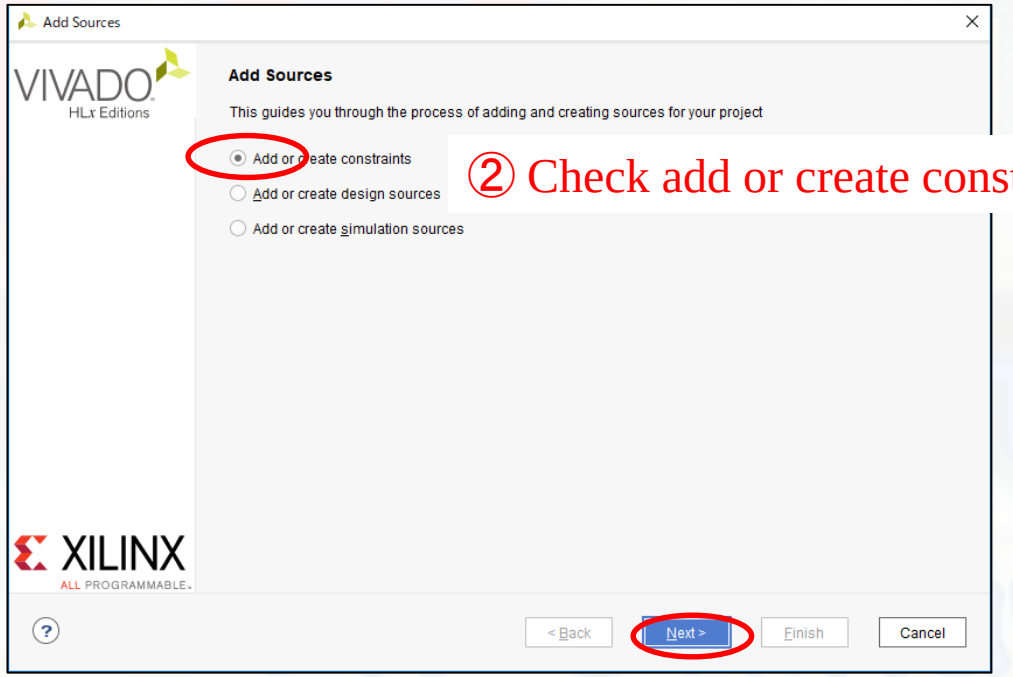


② Click OK, then Finish

Add constraints file

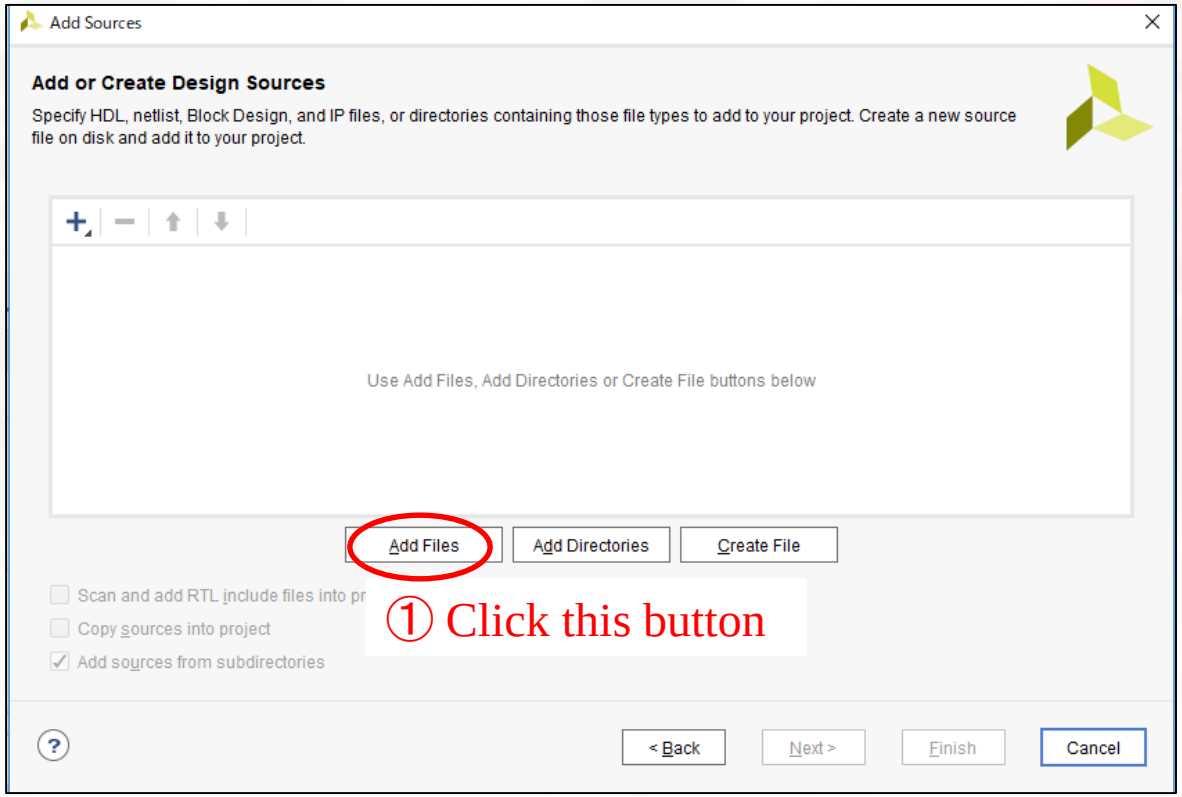
- Click Add source





Add source file

- Click Add files

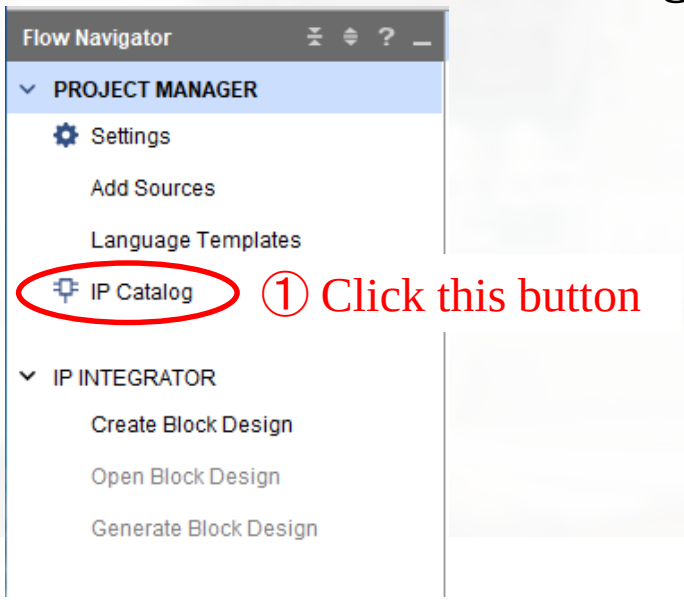


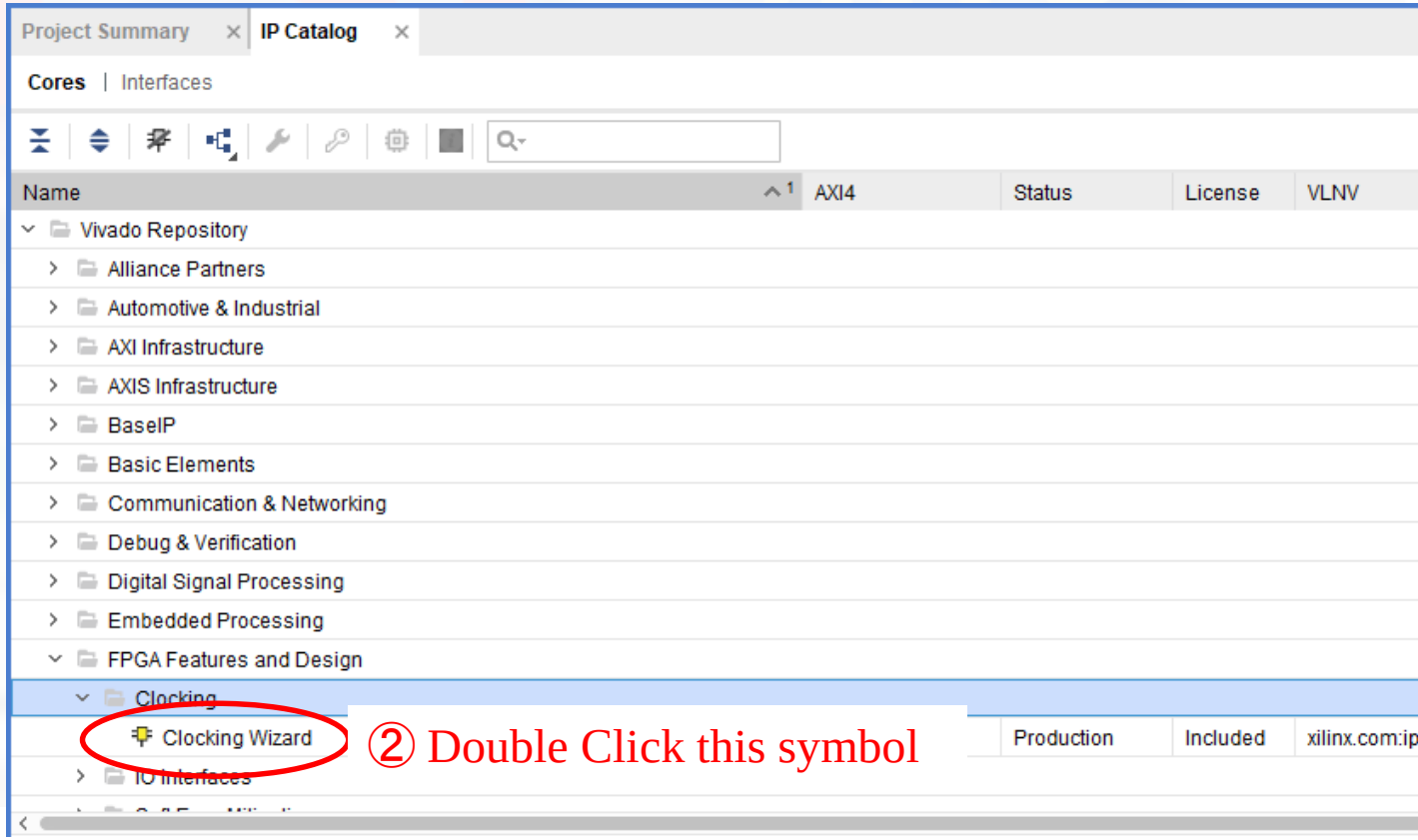
① Click this button

② Select design Constraint files (NN_top_zybo.xdc)
③ Click OK, then Finish

Add clocking wizard

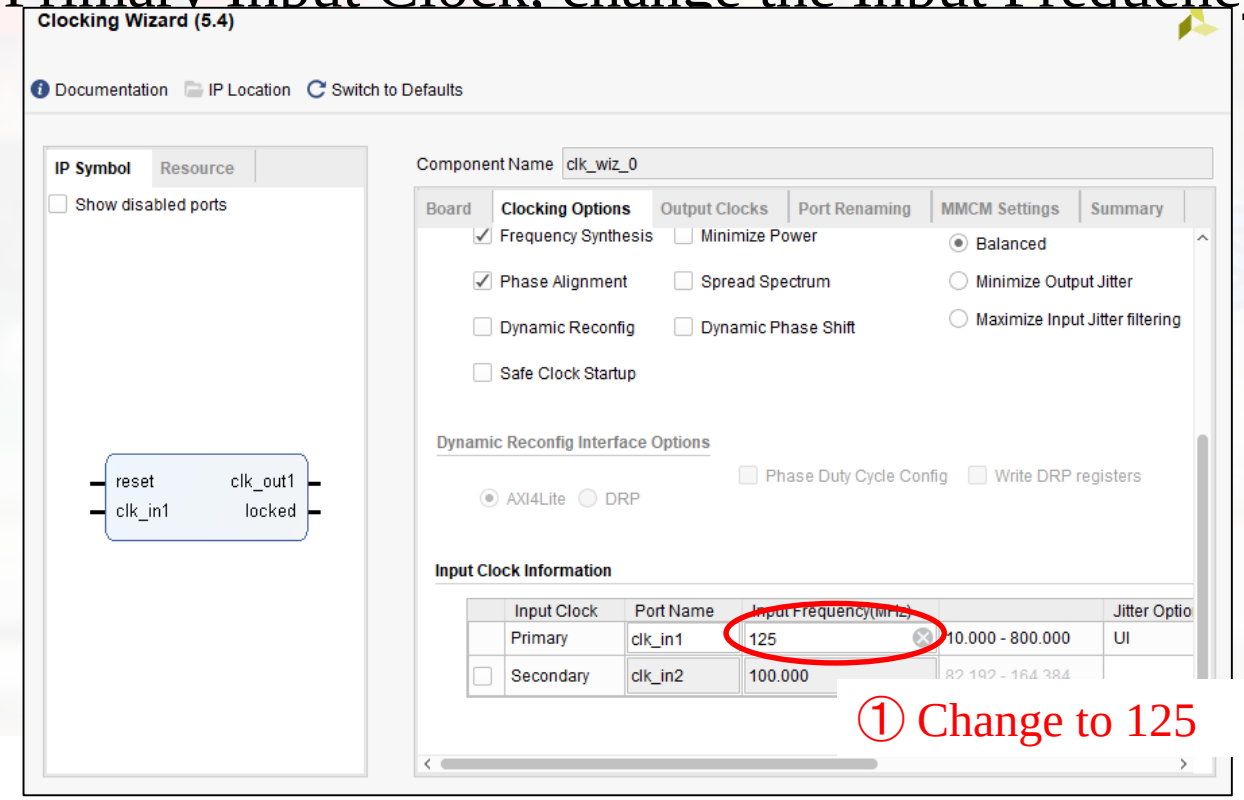
- Click the IP Catalog below PROJECT MANAGER
- In the IP Catalog window, expand FPGA Features and Design
  - Then expand Clocking
  - Double click the clocking wizard





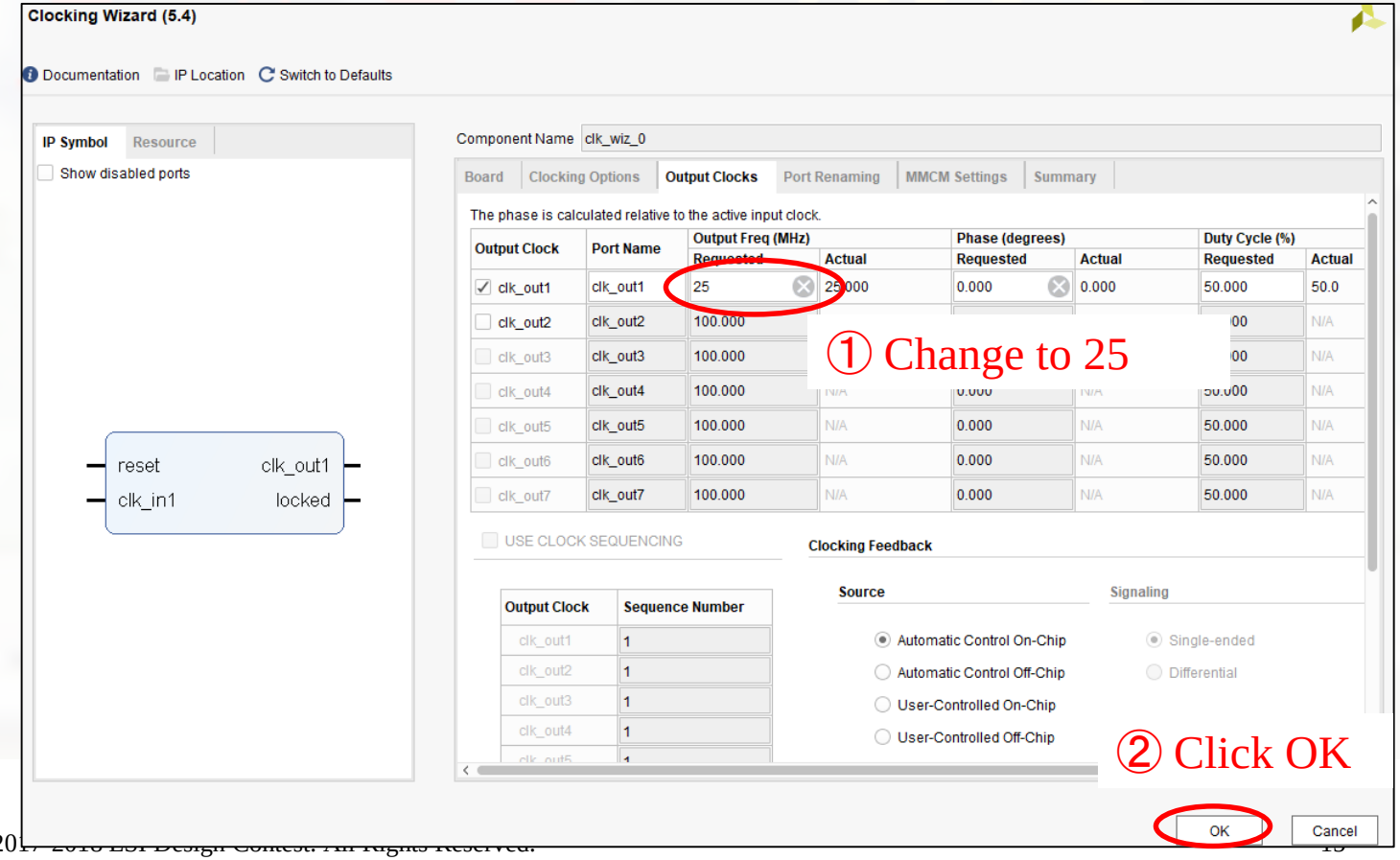
Add clocking wizard

- Customize IP window will open
- Open the Clocking Options tab
  - At the Input Clock Information, for Primary Input Clock, change the Input Frequency to 125 MHz



Add clocking wizard

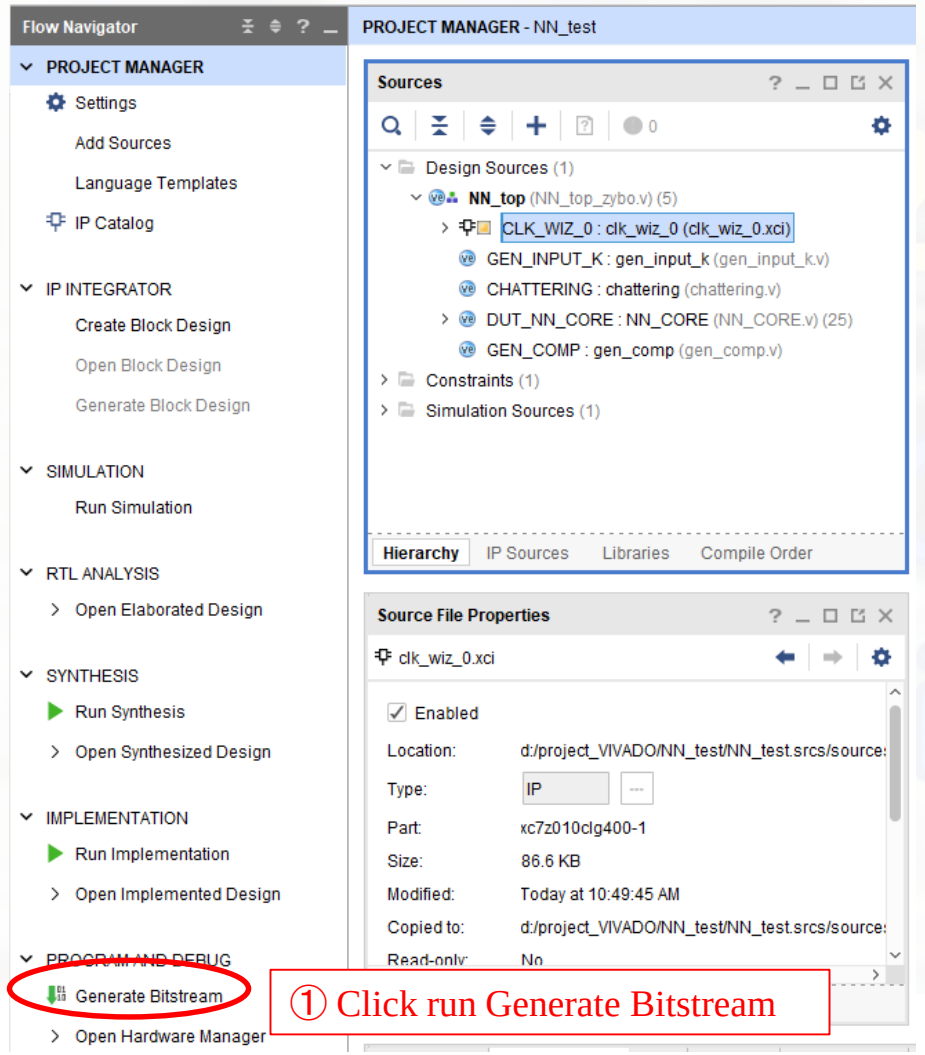
- Open the Output Clocks tab
  - At the Output Clock, change the Requested Output Freq to 25 MHz
- Click OK

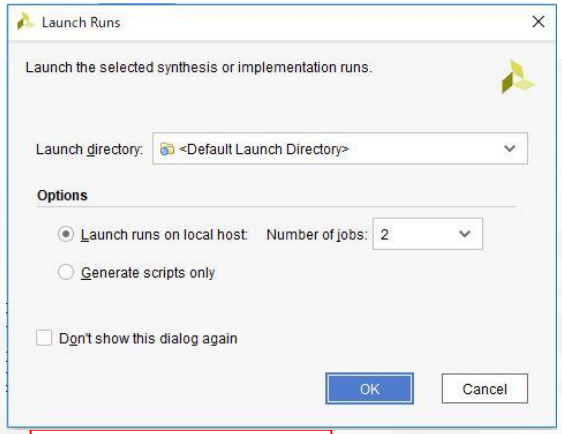


Generate Bitstream

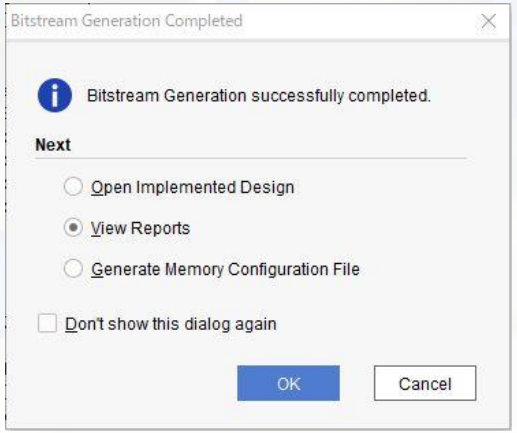
- In Flow Navigator, select PROGRAM AND DEBUG
  - Click Generate Bitstream

- When you program device, you should turn on board.





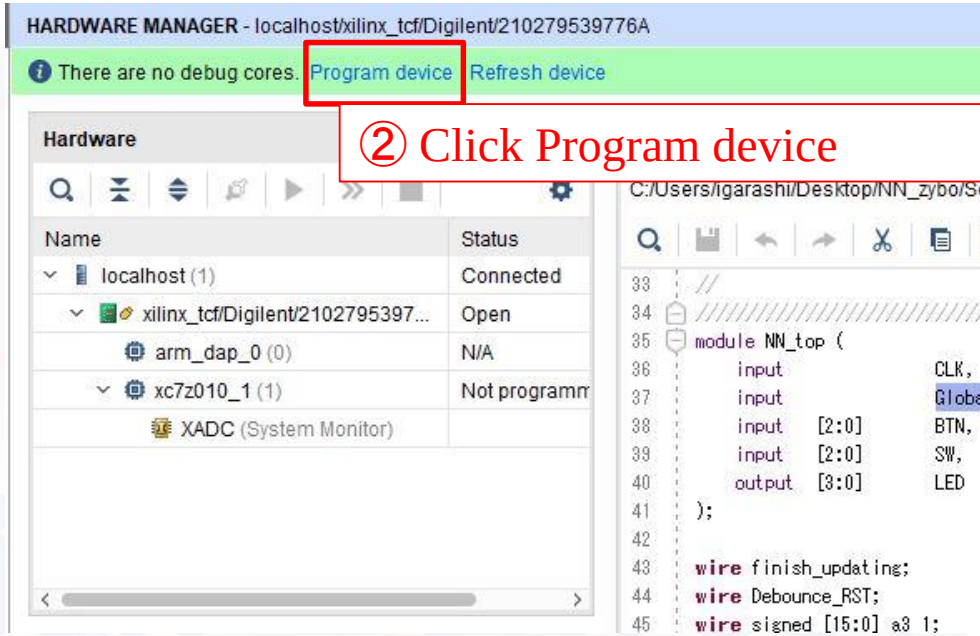
② Click OK



③ Click Cancel

Program the device

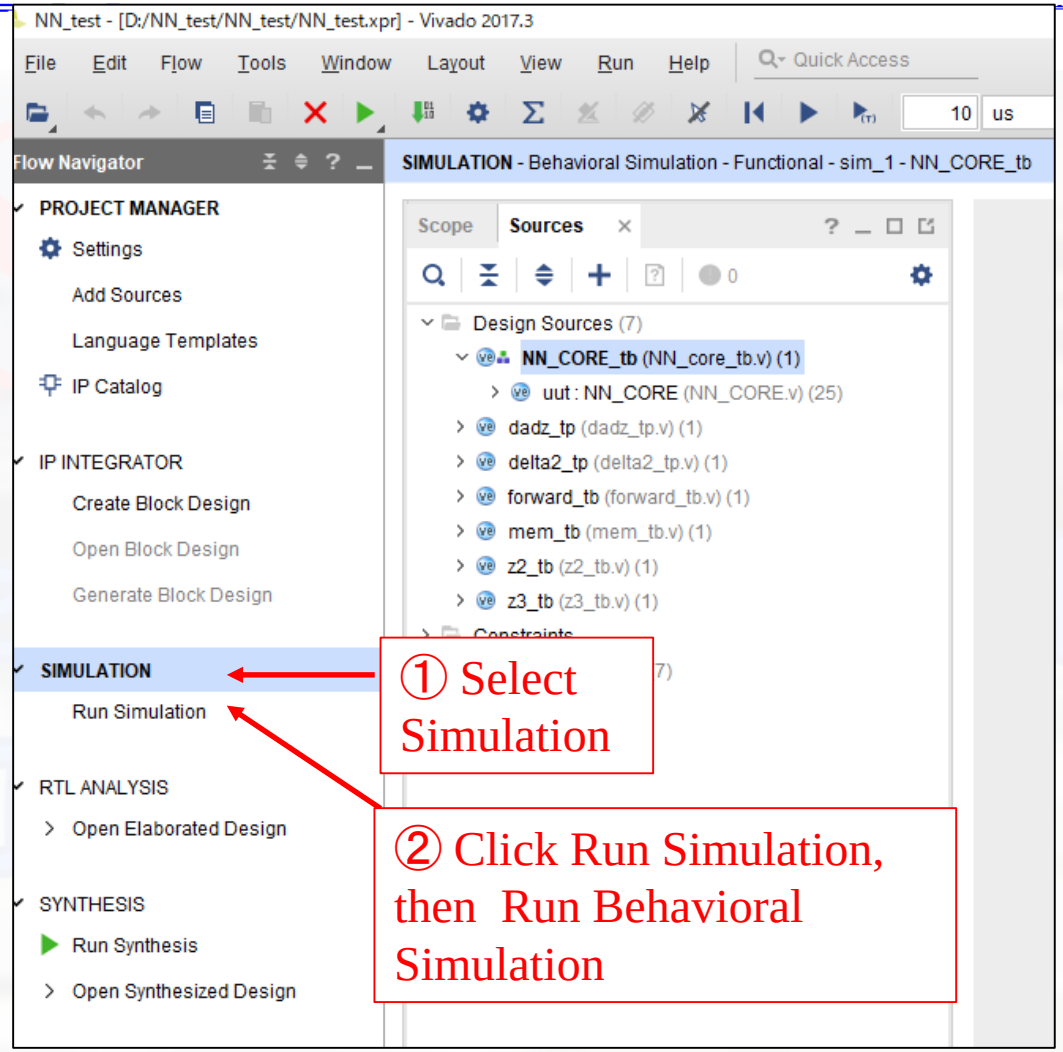
- Connect your board to your PC and turn on your board
- Expand the Open Hardware Manager below the Generate Bitstream
- Click Open Target and click auto connect



① Click Auto Connect

Simulate the project

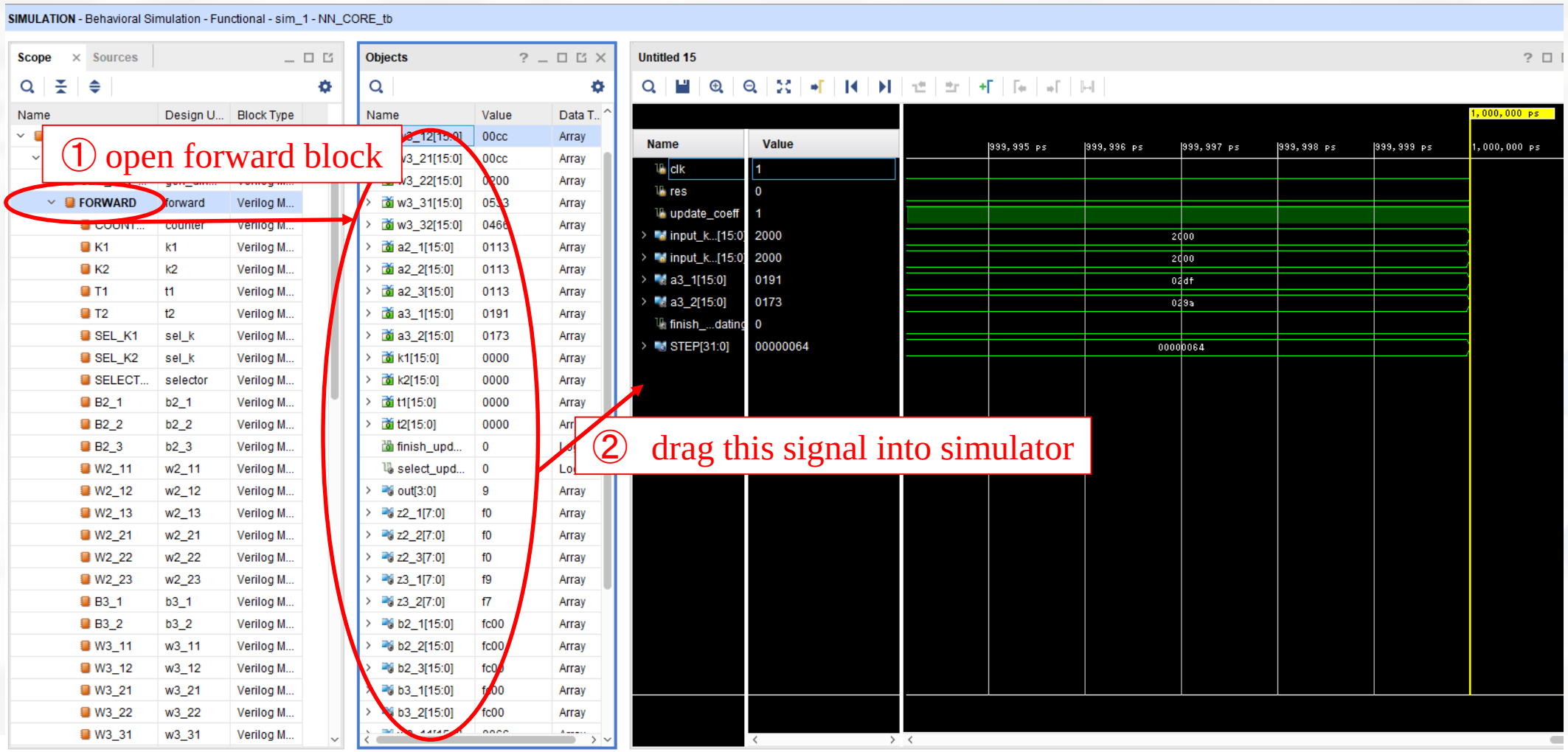
- Select Simulation
- Click Run Simulation
  - Click Run Behavioral Simulation



Vivado Simulator

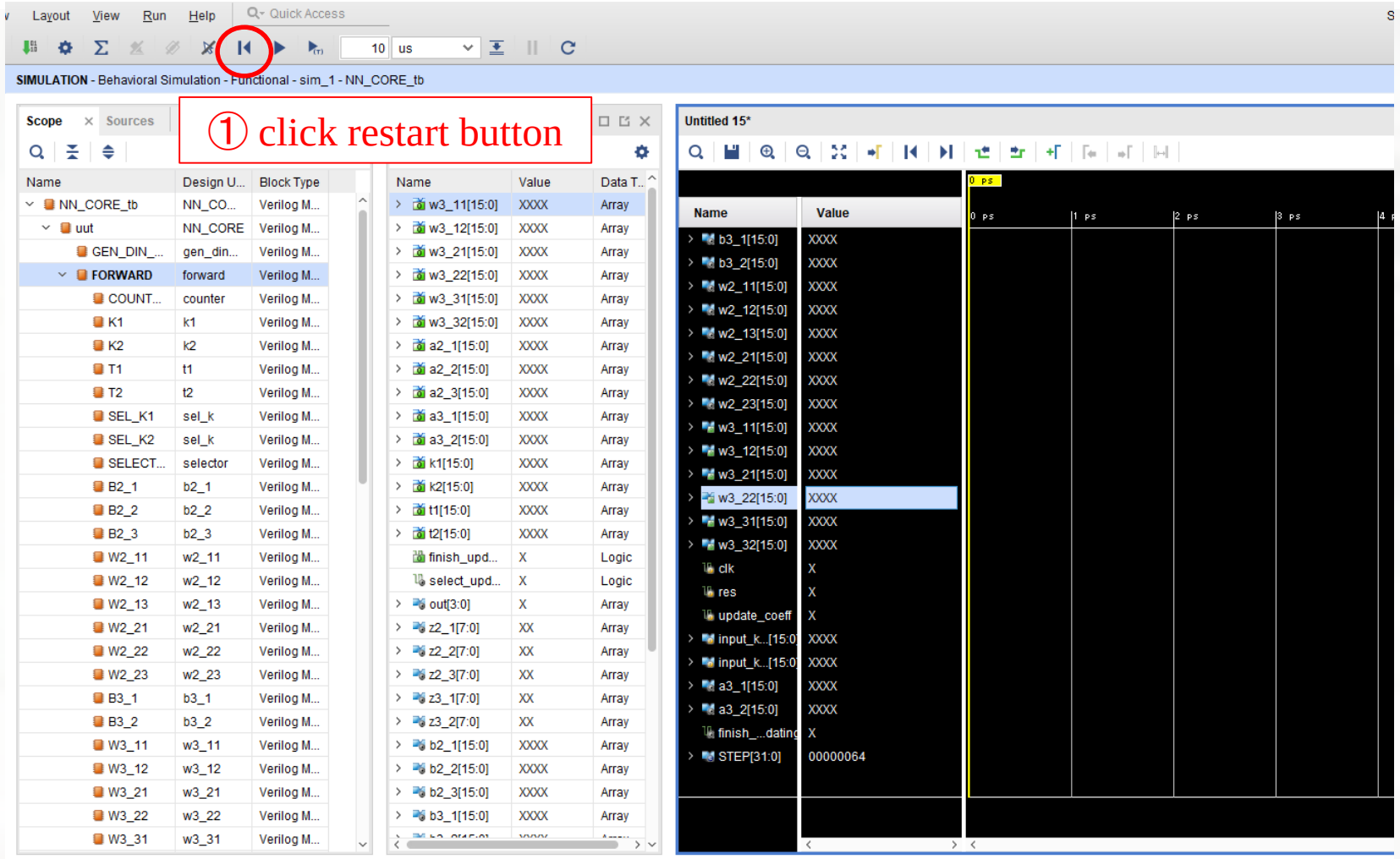
- Vivado simulator will open
- Choose forward block in Scope
  - Choose signal b2_1 until w3_32
  - Drag the signal into simulator
- Choose forward > selector block in instance and process name
  - Choose signal enable update
  - Drag the signal into simulator
- See the figure in the next slide…

Vivado Simulator



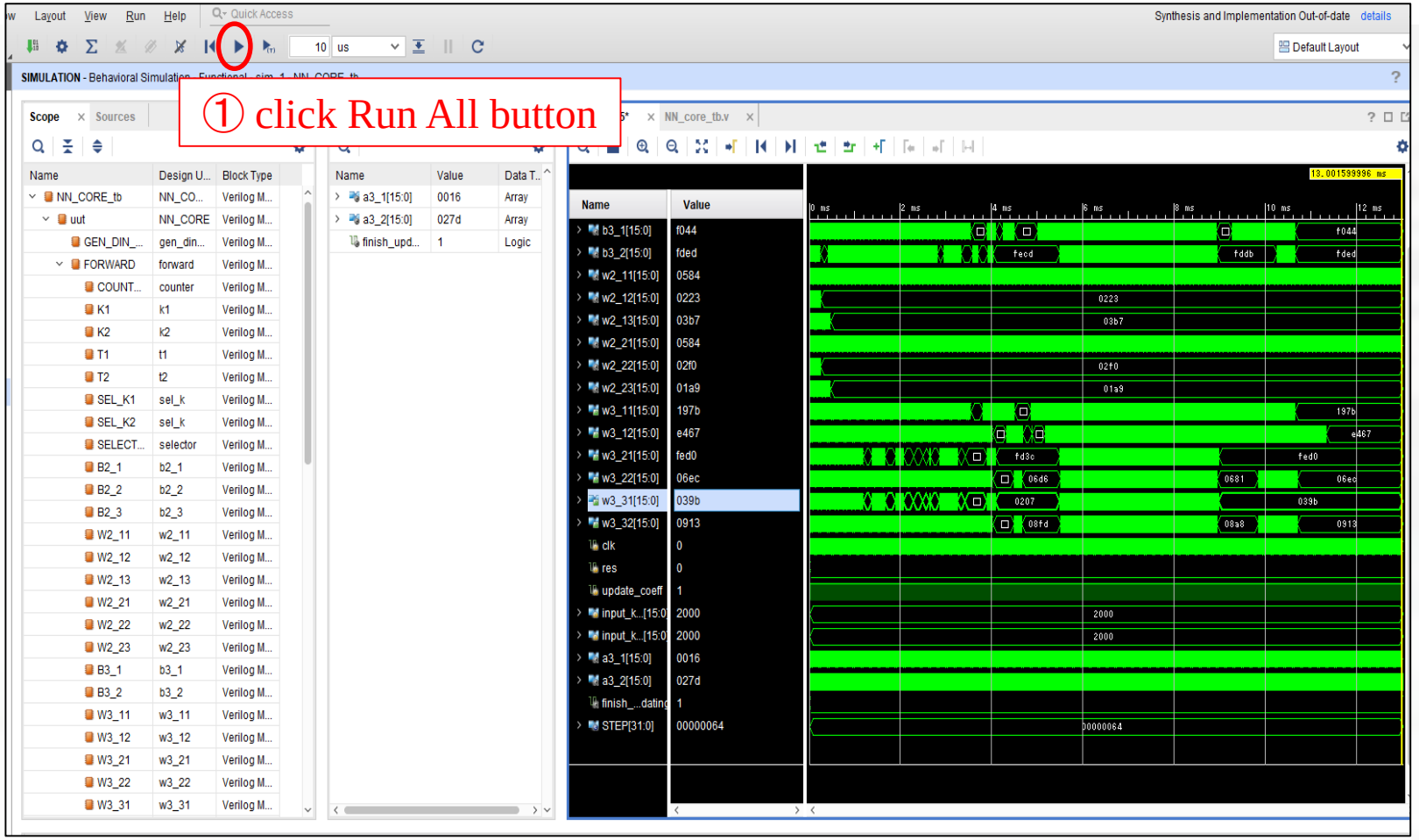
Vivado Simulator

- Click the restart button



Vivado Simulator

- Click the Run All button



Conclusion

- New weight and bias will be updated every time the enable update signal is active.